

M. MAHDI GHANDI

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Summary

I am a video coding expert with over 9 years of continuous focus on image and video coding, processing and communications from different aspects. I have developed many industry-standard software pieces for various projects mainly in C codes. I also have extensive experience in hardware design of video codecs in Verilog and VHDL. Customer support and project management are my other skills. I have shown that I am a hard-working engineer who learns new technologies and get up to speed very quickly – this can be confirmed by all my employers.

Work Experiences

Jan 2006 – Now, 4i2i Communications Ltd. (4i2i.com), Design Engineer – Project Manager

Main task: To design and engineer video coding IP cores for FPGA, ASIC and DSP applications.

Selected activities, projects, achievements and skills acquired:

- Serving as the key engineer responsible for 4i2i's H.264 decoder IP core which has been employed by several high-profile companies in broadcast, telecommunications and aerospace industry in their video systems.
- Project management of a group of engineers in various projects related 4i2i's H.264 decoder IP cores, including project planning, setting the deadlines, being responsible for meeting the deliverables.
- Direct customer support in integration of the delivered IP cores in various hardware systems. This includes meetings and conference calls with customers. The target systems include Xilinx and Altera FPGAs, and ASIC. Most of the target applications have been the broadcast industry.
- Design and development of High-Profile and High-422 profile H.264 decoder hardware cores using Verilog and VHDL languages. The cores have been tested in Xilinx V4 and V5, and Altera Stratix II and III evaluation platforms. Also, extensive functionality and performance tests for high-definition video decoding are conducted.
- Design and development of codec's efficient driver software in C language. My codes have been compiled in different systems including in Altera's NIOS and Xilinx's uBlaze processors.
- Design and development of fast and efficient variable-length encoding and decoding algorithms, namely H.264 CABAC and CAVLC encoder and decoder, mainly in Verilog.
- Engineering the decoder's error handling in hardware (Verilog) and software. This includes syntax error detection, and pixel error concealment.
- Engineering and maintenance of the core infrastructure, including ram interface, clock management, host programming, dma, etc.

- Interviewing engineering candidates when joining the company, and mentoring other engineers and colleagues in the office.
- Extensive use of tools such as Modelsim for hardware simulation, Synplify for synthesis, ISE for synthesis and place and route, Quartus for synthesis and place and route, MS visual C++ for C programming, Perl for scripting the tests, Linux shell-script and makefile for other scripting, SVN and MS Source-Safe for version control.

Jan 2003 – Dec 2005, University of Essex (essex.ac.uk), Senior Research Officer

Main task: To develop packet distribution algorithms for layered video transmission over wireless systems.

Selected projects, achievements and skills acquired:

- Research and development of novel video communication algorithms and presenting them in 6 prestigious scientific journals and more than 10 international conferences.
- Developing layering and scalability algorithms for robust transmission of H.264 video over mobile wireless channels – algorithms such as: 1- a new SNR scalability for H.264, 2- layered video transmission with HQAM, 3- Error concealment, 4- packet rearrangement and retransmission strategies, 5- using Turbo Coding for FEC, 6- Lagrangian optimizations.
- Developing general software tools (with visual C++) for playback and quality analysis of video streams with various types (H.263, H.264, YUV, AVI) for research purposes.
- Technical cooperation with many academic institutions, conferences and journals (joint research publications and peer reviewing several papers).
- Electronics and communication systems design and simulation using e.g. MATLAB.
- Developing an H.263++ codec in visual C++ supporting many H.263++ new annexes.

Dec 2001 – Dec 2002, Mir Gostar Farda Co., R&D Engineer/Project Manager

Project Management of software/hardware development projects.

- Developing (i.e. design, assembly programming, PCB, with OrCAD, Protel, Pspice) a microcontroller based analog electronic measurement device.
- Supervising four projects including: 1- A clinic management software (which is now profitably marketed), 2- A database website, and 3- Two measurement and microcontroller circuits design.

March 2000 – Dec 2001, Mabna Pardaz Rayaneh Co. (mabnapardaz.com), R&D Engineer

Design and development of image and video coding and processing tools.

- Implementation of fast and low complex JPEG2000 and MPEG codecs for TI C5x DSPs – speed and memory optimization of Ansi C codes.
- Research and developing a tool capable of editing, transcoding, picture resizing, and texture manipulating the MPEG video in compressed domain for Leitch video servers (acting as the team leader of four R/D engineers).
- Research and developing a new wavelet-based video codec for Leitch Inc., Toronto, Canada – it outperformed MPEG-2 and H.263 codecs, bonus was given and a patent was

filed.

- Software design and implementation using e.g. ANSI C, C++, visual C++, VB and assembly.

1998-2000, Iran Communication Industries Co., R&D Engineer (part-time)

Participating in a 10K telephone switch design project: design, simulation, PCB, and testing of microcontroller-based analog and digital electronic systems, e.g. switching power supply.

1997-1998, Machine Sazi Vije Co., Electrical Engineer (part-time)

PLC and control algorithm design, industrial electrical design with AutoCAD.

1996-1997, Iran Telecommunication Research Center (itrc.ac.ir), R&D Trainee (part-time)

Electronic circuits and system design for switching telephony systems.

Education

Jan 2003 – Jan 2006 PHD in Electronic Systems Engineering (part-time)

University of Essex, Colchester, UK.

Research thesis: Layered Video Coding for Wireless Communications.

Supervisor: Professor Mohammed Ghanbari.

Key skills acquired: The philosophy of research, Effective written and oral presentation, Supervision of projects, Advanced video coding, Error resilient wireless communications.

Oct 1999 – July 2001 M.Sc. in Electronics Engineering

University of Tehran, Tehran, (The most prestigious university in Iran) *Overall Grade:* 80%.

Research Thesis: Compressed Domain Processing of MPEG Video. *Grade:* 97%.

Supervisor: Dr Omid Fatemi.

Key skills/knowledge acquired: Basics of image and video processing, Advanced VHDL programming, Digital Signal Processing, Integrated low power circuits design, Data converters.

Oct 1994 – July 1998 B.Sc. in Electronics Engineering

University of Tehran, Tehran, Iran *Overall Grade:* 70%.

Supervisor: Dr Shahrokh Farhangi..

Project Report: A Sine Wave DC-AC Power Converter, Design/Implementation.

Project-Grade: 95%.

Key skills/knowledge acquired: Basics of electronics design, Advanced computer programming, Digital Circuits, Analogue Electronics design.

July 1994 Iranian Diploma in Mathematics

Nikan high school, Tehran, (One of the best schools in Iran for talented students) *Grade:* 85%.

General Skills, Qualifications, and Interests

- Enthusiastic about working in a team with excellent records of interaction with other colleagues.
- Project Management qualification from Learning Partnership, University of Essex, UK.
- Excellent written and oral presentation and communication skills, English IELTS: 8.
- High grade qualifications in swimming coaching, and life guarding. An ex-member of Tehran University swimming team (1994-2001) with several medals and honors.

- Interested in outdoor activities and sports such as mountaineering, rock climbing, rowing, canoeing, fencing, tennis, table tennis, badminton, volleyball, and football.
- A member of Aberdeen's CTM-B table tennis team. Won two trophies in 2008.

Selected Publications (*Full list available at <http://mahdi.ghandi.ws>*)

- M. Mahdi Ghandi and M. Ghanbari, "Layered H.264 video transmission with hierarchical QAM," Elsevier J. Visual Commun. Image Representation, Special issue on H.264/AVC, vol. 17, no. 2, pp. 451 - 466, April 2006.
- M. Ghandi and M. Ghanbari, "Error concealment for SNR scalable video coding," Elsevier J. Signal Processing: Image Commun., vol. 21, no. 2, pp. 91-99, February 2006. (the most downloaded article in Jan-March 2006).
- M. Ghandi, B. Barmada, E. Jones, and M. Ghanbari, "H.264 layered coded video over wireless networks - channel coding and modulation constraints," Eurasip J. Applied Signal Processing, Special issue on H.264/AVC, in press, to appear in 2006.
- Bashar Barmada, M. Mahdi Ghandi, Ed V. Jones, Mohammed Ghanbari, "Combined Turbo Coding and Hierarchical QAM for Unequal Error Protection of H.264 Coded Video," Elsevier J. Signal Processing: Image Commun., Jan. 2006.
- Bashar Barmada, M. Mahdi Ghandi, Ed Jones, and Mohammed Ghanbari, "Prioritized transmission of data partitioned H.264 video with hierarchical QAM," IEEE Signal Processing Lett., vol. 12, no. 8, pp. 577-580, Aug. 2005.
- M. Ghandi and M. Ghanbari, "The H.264/AVC video coding standard for the next generation multimedia communications," J. Iranian Association Elec. Eng., vol. 1, no. 2, pp. 3-14, Fall 2004.
- M. Ghandi, B. Barmada, E. Jones, and M. Ghanbari, "Unequally error protected data partitioned video with combined hierarchical modulation and channel coding," IEEE Int. Conf. Acoustics, Speech, Signal Processing, ICASSP, to appear in 2006.
- M. Ghandi and M. Ghanbari, "Robust video transmission with an SNR scalable H.264 codec," Proc. 7th IEEE Int. Conf. High Speed Networks Multimedia Commun., HSNMC, pp. 932-940, June/July 2004.
- M. Ghandi and M. Ghanbari, "A lagrangian optimized rate control algorithm for the H.264/AVC encoder," Proc. Int. Conf. Image Processing, ICIP, vol. 1, pp. 123-126, Oct. 2004.
- Compressed domain spatial scaling of MPEG video sequences ICCE 2002.

References (*to be contacted only with my consent.*)

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